M Ahmed Naveed 2022-EE-168

**Digital System**

Experiment 4

Combinational Circuit Design: RGB LED using K-Maps

Truth table

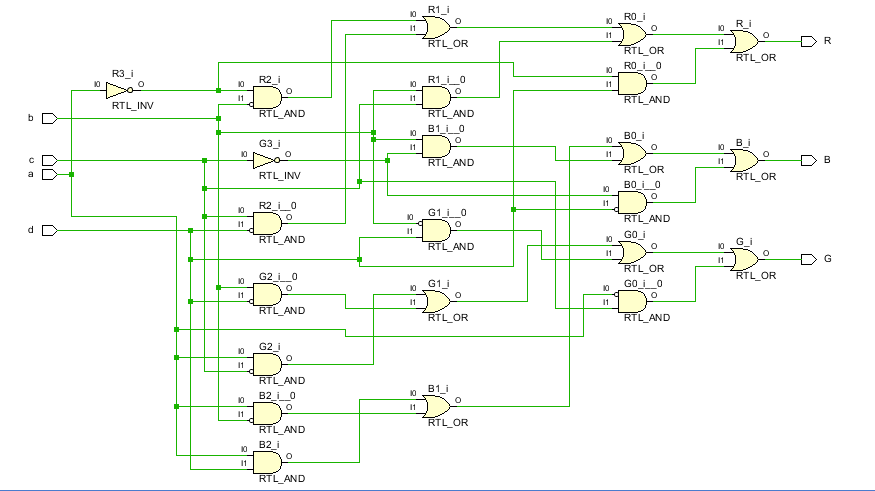
|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Input A | | Input B | | Output | | | Color |
| A | A1 | B | B1 | R | G | B |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | Purple |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | Yellow |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | Yellow |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | Yellow |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | Cyan |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | Purple |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | Yellow |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | Yellow |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | Cyan |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | Cyan |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | Purple |
|  | 0 | 1 | 1 | 0 | 1 | 1 | Yellow |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | Cyan |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | Cyan |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | Cyan |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | Purple |

K-Map

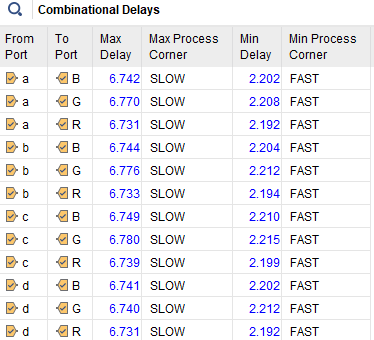
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | |  | K map for R | | | | | | |  |  | 00 | o1 | 11 | 10 |  | |  | 00 | 1 | 1 | 1 | 1 |  | |  | 01 | 0 | 1 | 1 | 1 |  | |  | 11 | 0 | 0 | 1 | 1 |  | |  | 10 | 0 | 0 | 0 | 1 |  | |  |  |  |  |  |  |  |

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| K map for G | | | | | | | | | | | |
|  |  | | 00 | 01 | | 11 | | 10 | |  |  |
|  | 00 | | 0 | 1 | | 1 | | 1 | |  |  |
|  | 01 | | 1 | 0 | | 1 | | 1 | |  |  |
|  | 11 | | 1 | 1 | | 0 | | 1 | |  |  |
|  | 10 | | 1 | 1 | | 1 | | 0 | |  |  |
|  |  | |  |  | |  | |  | |  |  |
|  |  | |  |  | |  | |  | |  |  |
| K map for B | | | | | | | | | | | |  |
|  | | oo | | | o1 | | 11 | | 10 | | |  |
| oo | | 1 | | | 0 | | 0 | | 0 | | |  |
| o1 | | 1 | | | 1 | | 0 | | 0 | | |  |
| 11 | | 1 | | | 1 | | 1 | | 1 | | |  |
| 10 | | 1 | | | 1 | | 0 | | 1 | | |  |

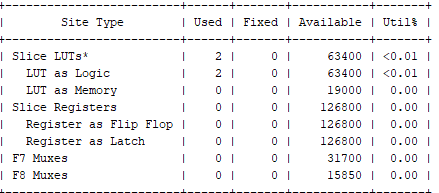
Circuit Diagram



Combinational Delay



Resource Utilization



System Verilog Code

module project4 ( input logic a,b,c,d,

output logic R,G

);

assign R = (~a && ~b) || (c && ~d) || ( b && c) || (~a && d) :

assign G = ( a && ~c) || (b && ~d) || (~b && d) || (~a && c);

assign B = ( a && d) || (a && ~b) || ( b && ~c) || (~c && ~d);

endmodule

vmodule project4\_tb();

a = 1; b = 0; c = 0; d = 0;

#10

a = 1; b = 0; c = 0; d = 1;

#10

a = 1; b = 0; c = 1; d = 0;

#10

a = 1; b = 0; c = 1; d = 1;

#10

a = 1; b = 1; c = 0; d = 0;

#10

a = 1; b = 1; c = 0; d = 1;

#10

a = 1; b = 1; c = 1; d = 0;

#10

a = 1; b = 1; c = 1; d = 1;

#10

$stop;

end

endmodule

logic a,b,c,d;

logic R,G,B;

project4 dut (

.a(a),

.b(b),

.c(c),

.d(d),

.R(R),

.G(G),

.B(B)

);

initial begin

a = 0; b = 0; c = 0; d = 0;

#10

a = 0; b = 0; c = 0; d = 1;

#10

a = 0; b = 0; c = 1; d = 0;

#10

a = 0; b = 0; c = 1; d = 1;

#10

a = 0; b = 1; c = 0; d = 0;

#10

a = 0; b = 1; c = 0; d = 1;

#10

a = 0; b = 1; c = 1; d = 0;

#10

a = 0; b = 1; c = 1; d = 1;

#10